REMARKS/ARGUMENTS

Claims 1-13 remain pending in this application and stand rejected. Claims 1, 8, and 9 are amended to clarify their respective inventions. The abstract of the disclosure is amended above to comply with MPEP 608.01(b) and to overcome the objection made by the Examiner. The attached formal drawings replace the original informal drawings of Figures 1-3.

The present invention is related to line build-out circuits that are wired communication lines as recited, for example, in claim 1. However, to further clarify this point, Claim 1 is amended to recite that the transmission line over which signals are transmitted is wired, and thus recites, in part, "...anticipated amount of signal degradation over a wired transmission line". Claims 8 and 9 are likewise amended

Claims 1-4 are rejected under 35 USC 102(e) as being anticipated by Shyue U.S. Patent No 6,359,936 B1 (hereinafter Shyue). In rejecting claim 1, the Examiner asserts:

"As per claim 1, Shyue teaches a digital line build out circuit comprising: a memory storing a plurality of digitized waveforms (se fgs. 4-6, 8a-8b elements 80 or 100 and col. 2, lines 5-6 and col. 6, lines 65-57 and col. 7, lines 1-20)' a selection circuit, coupled to said memory, to select (see figs 4-6, 8a-8b elements 74,184, 200, 284 and col. 9, lines 10-25 and col. 10, lines 43-67) certain ones of said waveforms corresponding to an anticipated amount of signal degradation over a transmission line; and a digital to analog converter (see element 44, and col.7, lines 13-20) to convert said certain ones of said waveforms into analog waveforms for transmission."

Applicants respectfully traverse this rejection. Shyue is directed to a modulator for use in cordless phones:

"...There are two important considerations in the design and implementation of cordless telephones..." (1:22-25)

"...Conventional cordless telephones employ transmitters that use a quadrature modulator, which is well known in the art ..." (1:41-43)

Accordingly, the modulator discussed in Shyue is not directed to wired systems. Therefore Shyue fails to disclose claim 1. Moreover, because the modulator discussed in Shyue is not directed to wired systems and is instead directed to cordless phones, memory 80, shown in Figs. 4-6, and memory 100 shown in Figs. 8A-8B do not store "digitized waveforms corresponding to different anticipated amounts of signal degradation over a wired transmission line", as recited in claim 1. In other words, memory 80, shown in Figs. 4-6, and memory 100 shown in Figs. 8A-8B of Shyue do not store digitized waveforms of signals to be transmitted over a wired transmission line. Claim 1 is this allowable over Shyue. Claims 2-4 are allowable over Shyue for at least the same reasons as is claim 1.

Claim 4 is allowable over Shyue for the following additional reason. In rejecting claim 4, the Examiner asserts:

"As per claim4 and 7, Shyne does include an adder or summer is the same as the claimed (a combining circuit) (see fig. 7 element 290 and col. 9, lines 37-40), coupled between said memory and said digital to analog converter, to combine a portion of a current digitized waveform with a portion of at least one previous digitized waveform."

Applicants respectfully traverse this rejection. Contrary to the Examiner's assertions, summation circuit 290 is a part of finite levels supplier 120, which in turn, is a part of non-linear DAC 44:

"FIG. 7 illustrates in greater detail the non-linear DAC 44 of FIG. 6. Non-linear DAC 44 includes a decoder 104 that is coupled to MUX 184 to receive signals Q[4 . . . 0] and a finite levels supplier 120 coupled to decoder 104. Decoder 104 decodes the received signals and provides control signals B[(L-1) . . . 0]. Finite levels supplier 120 includes a plurality of voltage or current suppliers 284 for supplying a voltage or a current, a plurality of switches 288, and a summation circuit 290. Each switch 288 is coupled to a respective voltage supplier 284 and generates an output. Each switch 228 also receives and is controlled by a respective control signal provided by decoder 104. Summation circuit 290 is

coupled to the voltage suppliers 284 for summing the outputs of the voltage suppliers 284. " (Fig. 7, col. 9, lines 29-42)

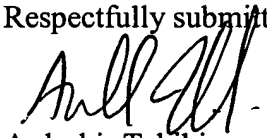
In other words, summation circuit 290 is used to convert digital signals to analog signals and not to "combine a portion of a current digitized waveform with a portion of at least one previous digitized waveform", as the Examiner mistakenly asserts. Summation circuit 290 of Shyue, therefore, fails to teach or suggest "to combine a portion of a current digitized waveform with a portion of at least one previous digitized waveform", as is recited , in part, in claim 4. Claim 4 is thus allowable over Shyue for this additional reason.

Claims 5-13 are allowable for at least the same reasons as is claim 1 and/or claim 4.

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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